Step By Step Learning Robei

I. Logic Gate Design

Robei LLC

1. Objective

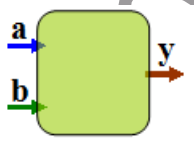
Logic gate is the fundamental of digital chip design. In this lab, we will analyze how to realize logic gate design and simulation with Verilog language in Robei. Through this lab, you will get familiar with Robei's "Graph+Code" design method in fast prototyping.

2. Prepare

2.1 And Logic

Common logic gates in digital design are AND, OR, XOR, NOT, NAND, NOR, XNOR etc. In this lab, we first discuss about AND gate then you can complete all the exercise for other logic gates. The truth table of AND gate shows in fig. 1, when both inputs a and b are high on voltage, the output is high. Mathematical equation for AND gate shows in Equation (1):

$$y = a \,\&\, b \tag{1}$$



a	b	y
0	0	0
0	1	0
1	0	0
1	1	1

Fig.1. AND gate logic and its truth table

2.2 Software

Please prepare yourself with Robei chip desgn software. You can download the latest version from:http://www.robei.com. After installation, you can open the software and get familiar with the software structure. There is a PDF version user guide for Robei if you click on menu: "Help" then click on "Help" in sub-menu.

3. Procedure

Robei LLC

Copyright © Robei

3.1 Module Design

1) Create a new module. Click on icon  in toolbar, or select drop-down menu “New” from menu “File”, a dialog will pop up shows in fig.2. You can set the properties of your design in this dialog.
2)

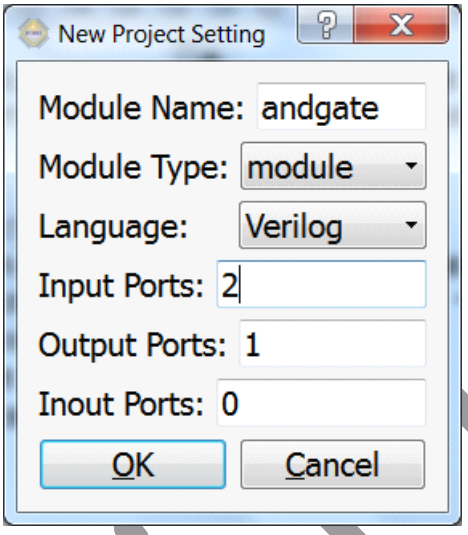


Fig. 2. New project

Elements in Fig. 2:

(1) Module Name: we want to create a module named “andgate”, then type “andgate”.

(2) Module Type: Robei supports 3 different types, “module”, “testbench” and “constrain”. Because we want to create a module, so just select “module”.

(3) Language: Verilog is the only choice.

(4) Input Ports: input ports number. In our design, there are only two input ports, so type 2.

(5) Output Ports: output ports number. We only need one here, so type 1.

(6) Inout Ports: inout ports number. In the design, we don’t need such type of port. So leave it 0.

After filling this dialog, press button “OK”, Robei will generate a new module with name “andgate” as shows in fig.3.

Robei LLC

Copyright © Robei

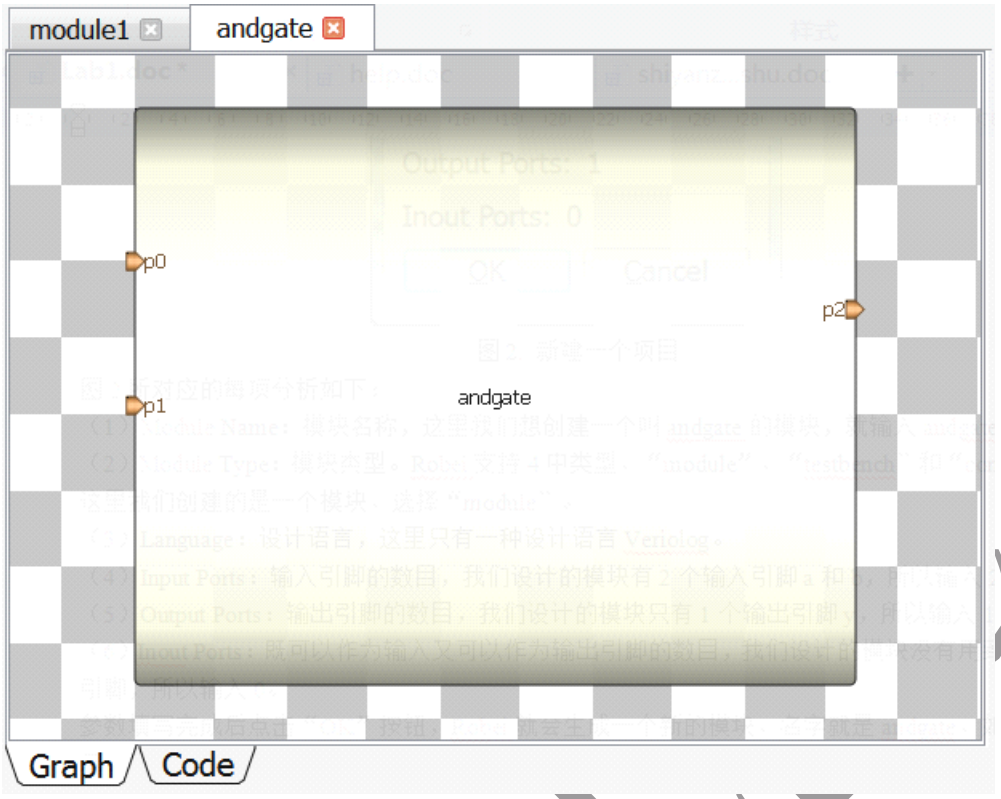
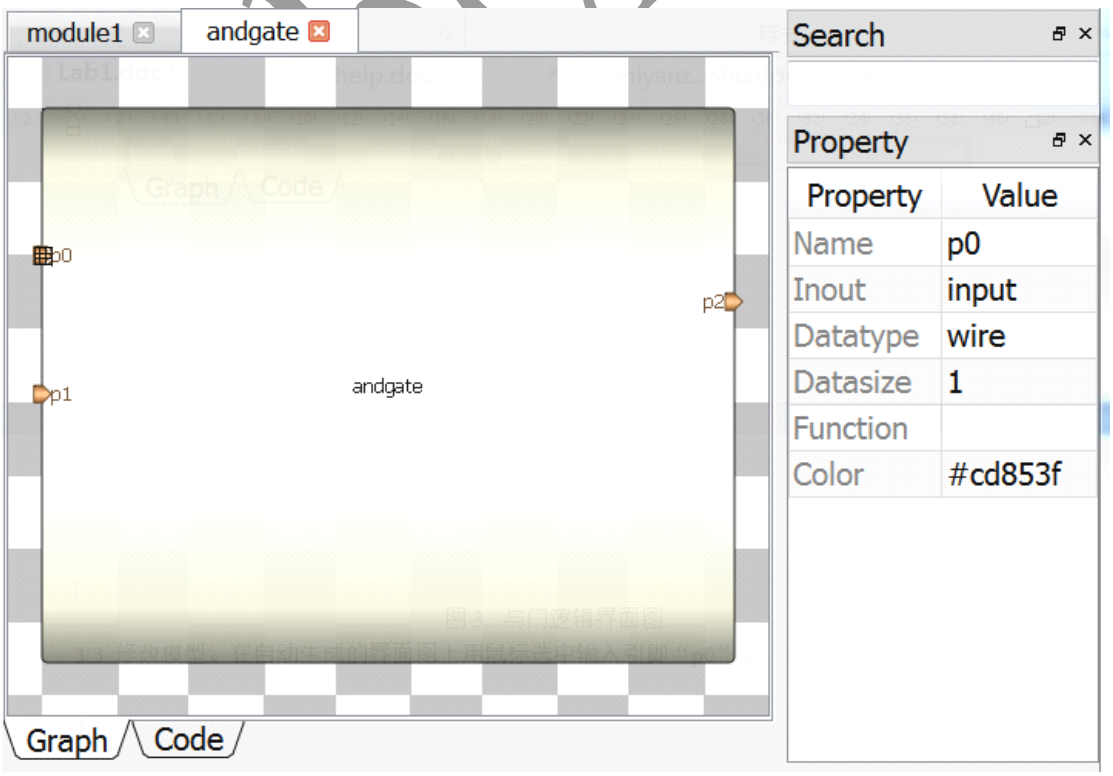


Fig. 3. AND gate graphical interface

3) Modification. Select “p0”, all the properties of this pin will show up in property editor. Please change name to “a” and change name of “p1” to “b”. After such modification, changes will directly show up in Graph when you press “Enter”. You can modify the color property of each pin to distinguish with each other.



Copyright © Robei

Fig. 4. Properties of “p0”

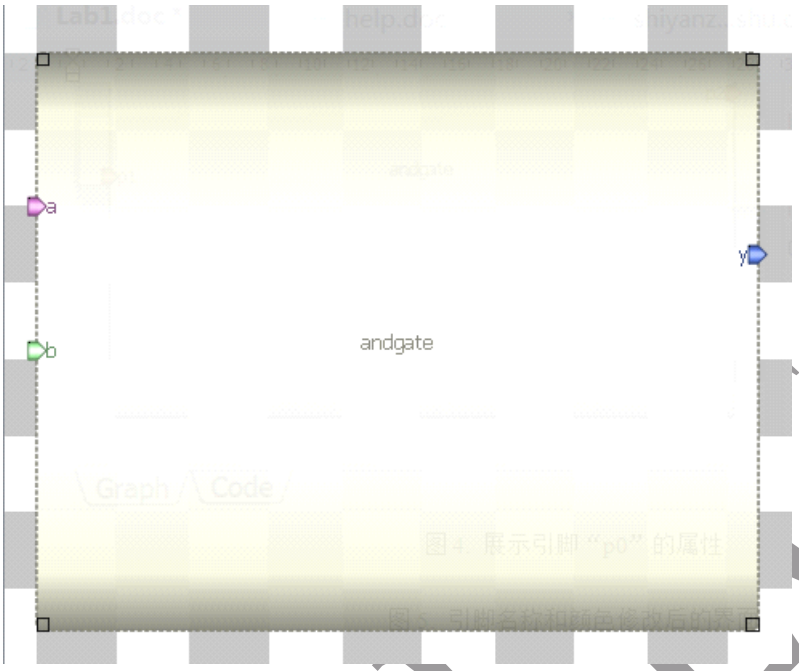


Fig. 5. Interface after color changing

4) Code algorithm. Click on the “Code” tab under module, code editor will show up for you to typing algorithm code for this module (shows in fig.6).

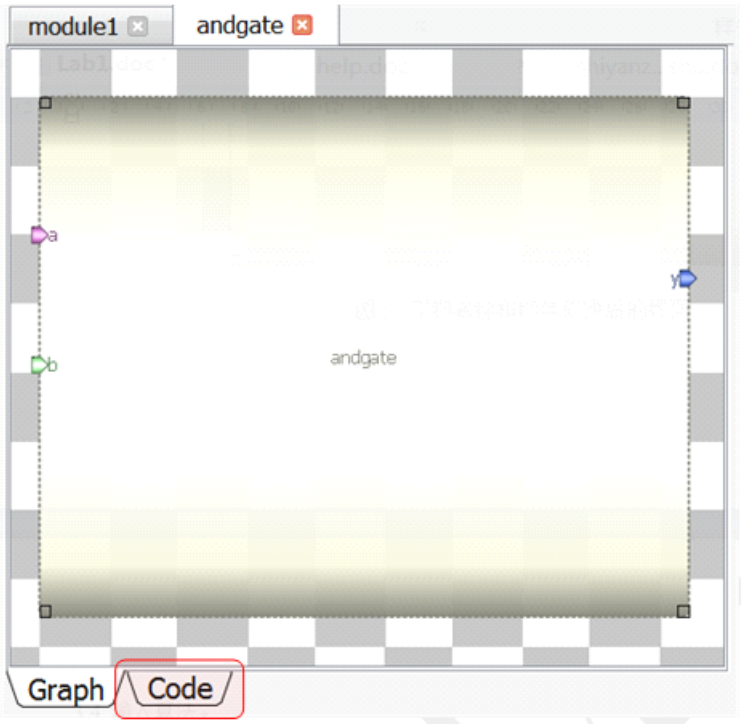


Fig. 6. Location of “Code” tab

In code editor, type the following code:

```
assign y = a & b;      // Learn how to write assign in Verilog.
```

Copyright © Robei

This line of code realized AND logic in digital design.

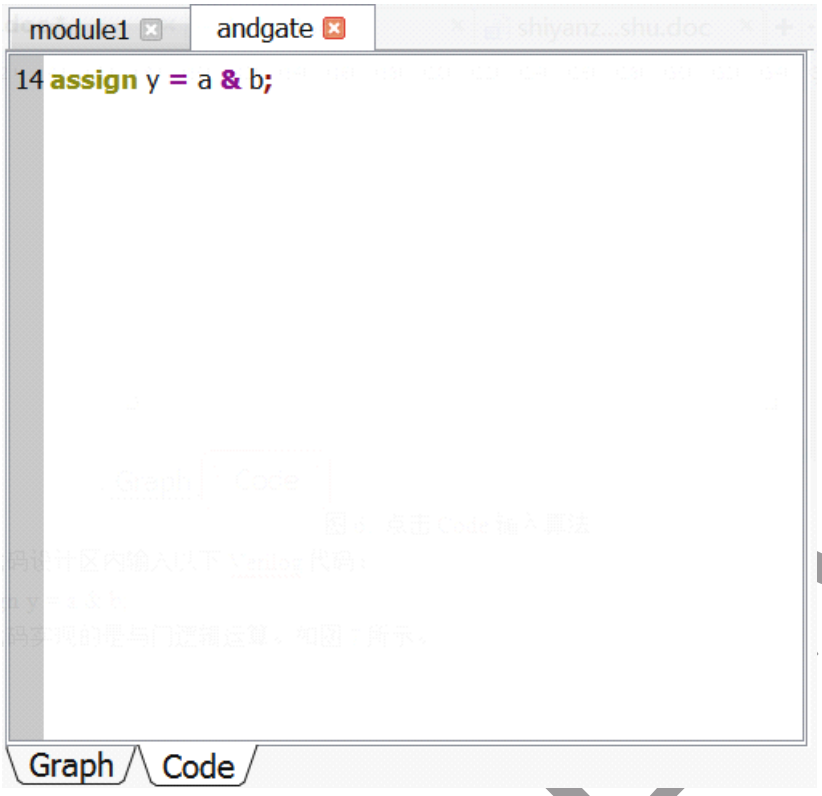


Fig. 7. Code editor

5) Save. Press icon  on Toolbar, or click on drop-down menu “Saveas” in menu “File”, save this model in an empty folder. Note: this empty folder can not have white space in path, and can only use English characters.

Robei

Copyright © Robei

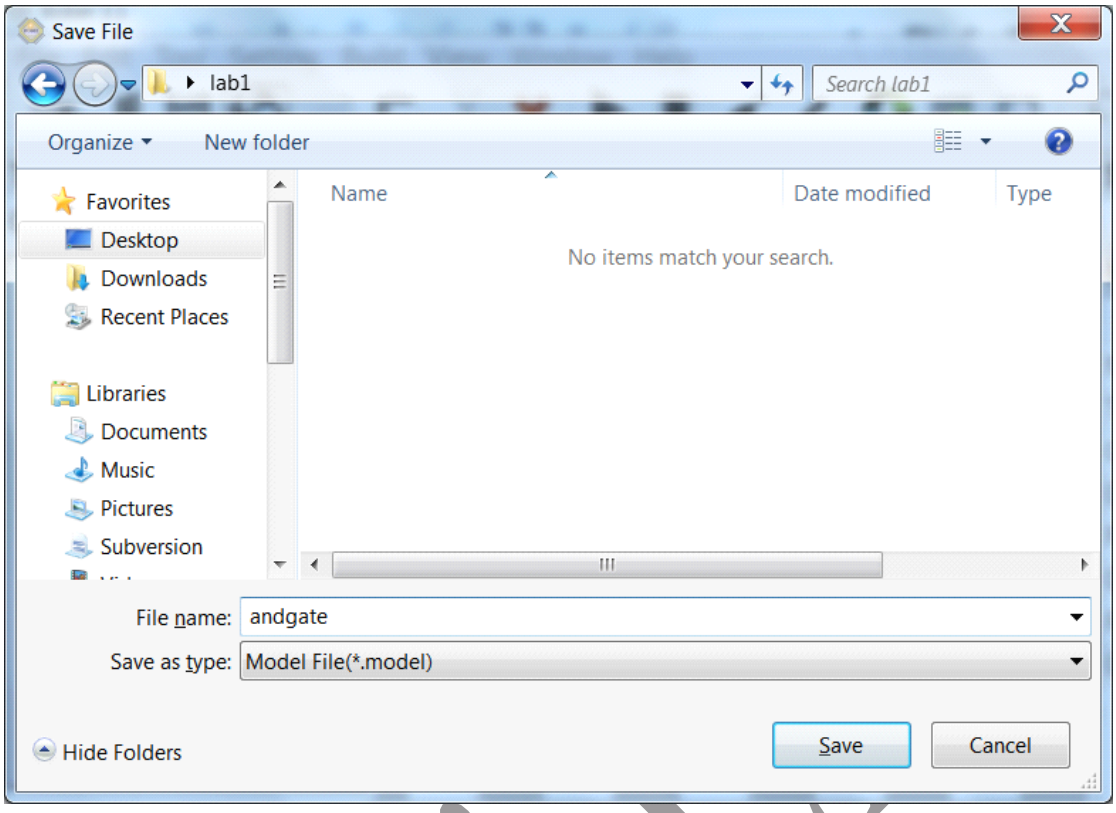


Fig. 8. Save as module

6) Run. Press on icon  or click on drop-down menu “Run” in menu “Build”.

In this process, Robei will generate complete Verilog code and check. If there is any error, it will show error message in Output window. Please follow the instruction to correct any errors. After that, congratulation, you have complete the first model design.

3.2 Testbench Design

1) Create a new design. Press on icon  in toolbar, in the pop up dialog, fill in blank with the following parameters in fig. 9.

Robei LLC

Copyright © Robei

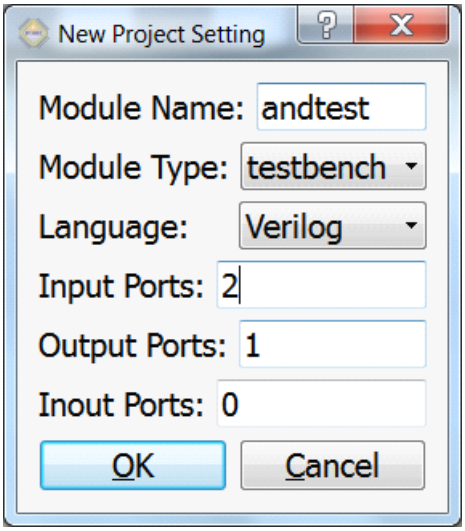


Fig. 9. Create a new testbench, “Module Type” must set as “testbench”

2) Modify color of ports. Select each port, modify color from property editor.

Fig. 10. Modify color

3) Save as testbench. Click on icon  in Toolbar, save testbench to the same location as “andgate” .

Copyright © Robei

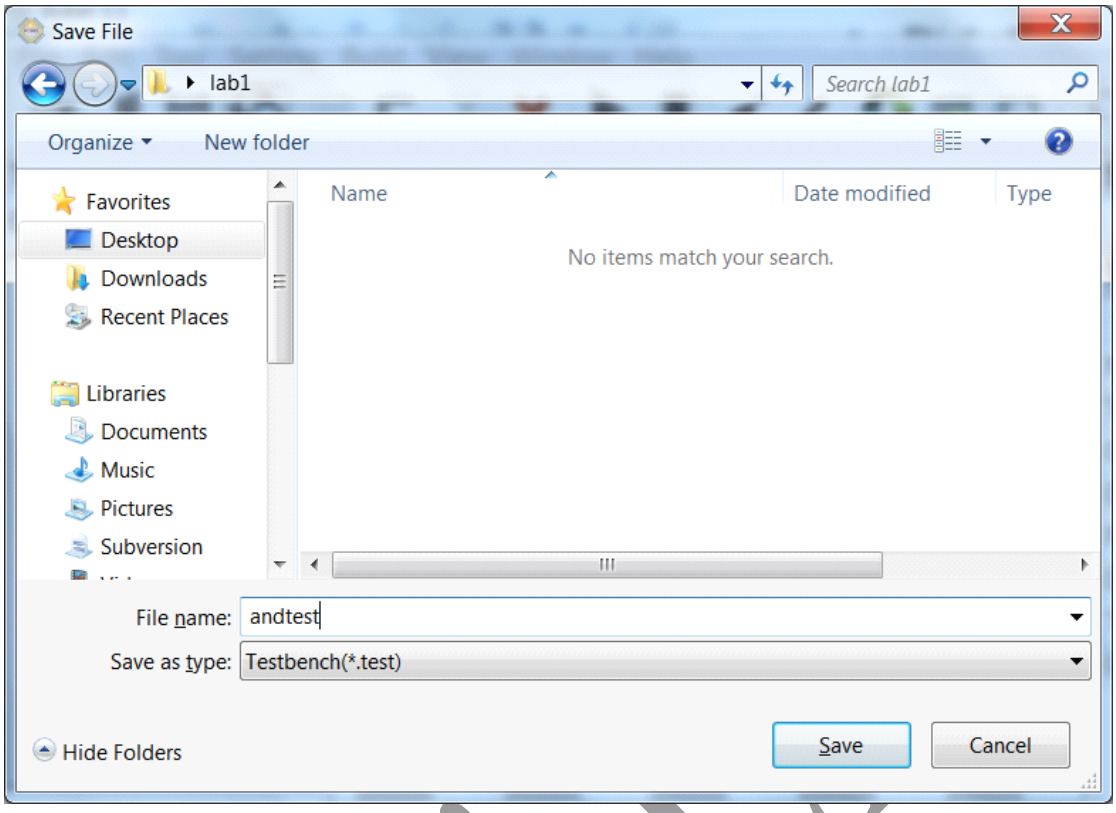


Fig. 11. Save as testbench

4) Add model. Under category "Current" in Toolbox, there will be one model show up as fig.12. Click on this model and click on the testbench design, Robei will add this model in automatic.

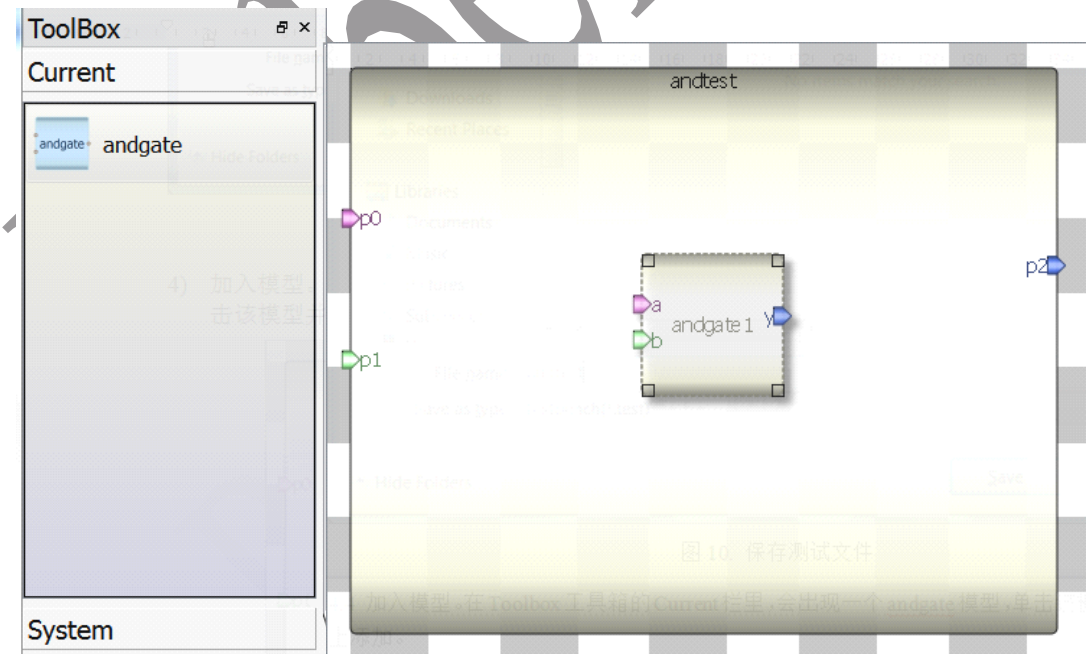


Fig. 12. Add model

Copyright © Robei

5) Connect ports.Click on icon  in Toolbar, or select “Connect” from menu “Tool”. Conect port p0 to a, p1 to b, y to p2. When you connect, remember to check the color of connection, as it will inherent from the first port directly. If you want to quit connection mode, press on icon  .

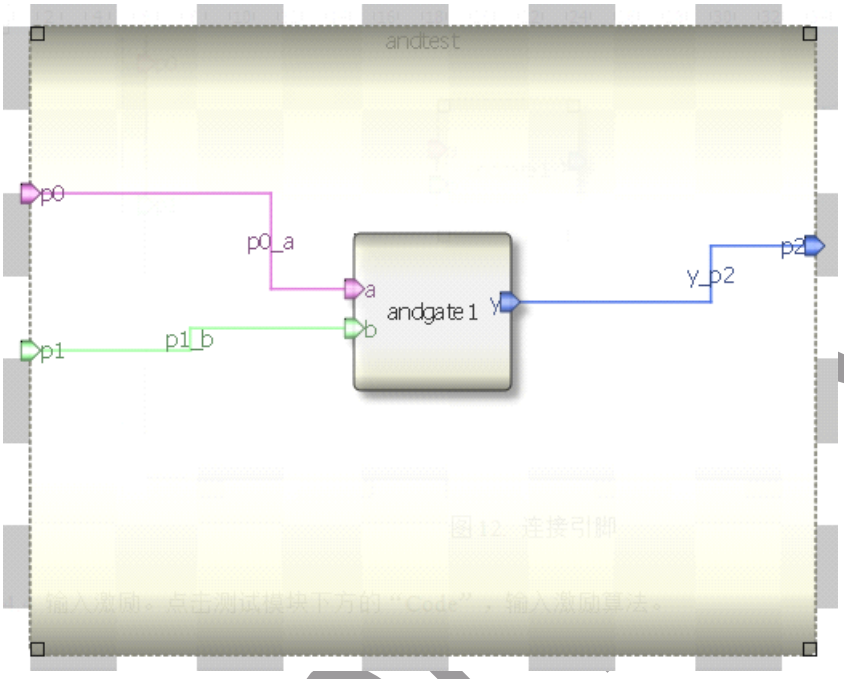


Fig. 13. Connect ports

6) Code stimulate. Press “Code” tab under testbech, type in the following code as stimulate for simulation. Remember to use $finish to end this simulation.

```
initial begin      // Learn how to write initial begin in Verilog
   p0 = 0;       //Set default value
    p1 = 0;
    #1           // One clock delay
       p0 = 1;
    #1           //Another clock delay
       p1 = 1;
    #1
       p0 = 0;
    #1
       p1 = 0;
    #1
       $finish;    //Simulation end flag
end
```

Robei

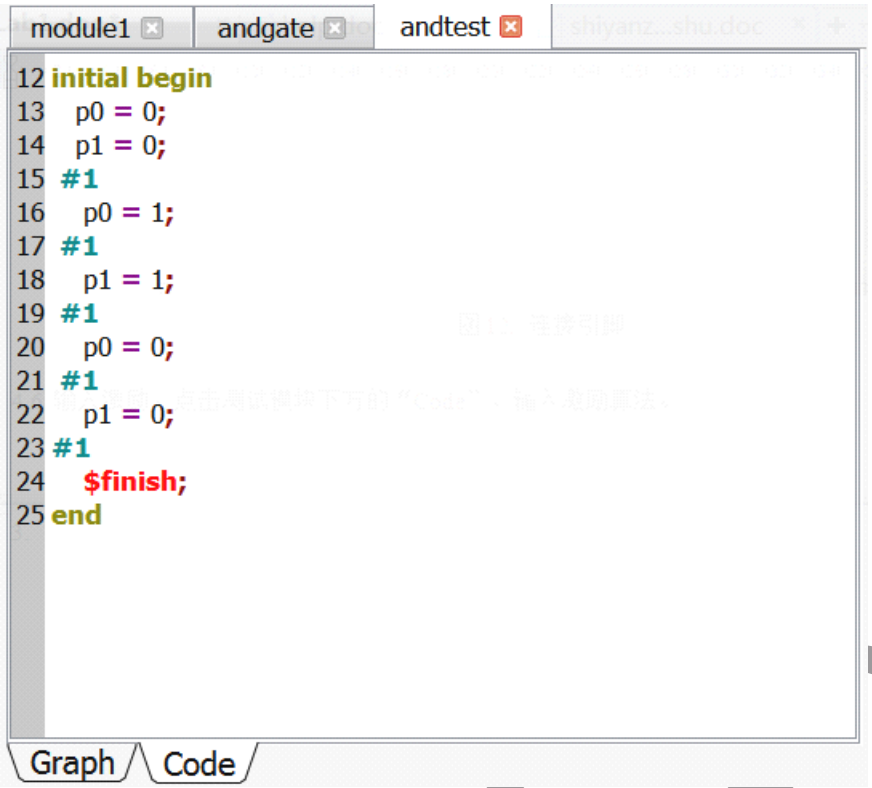


Fig. 14 Stimulate code

7) Run simulation and check the waveform. Click on  , check output information, if there is no error, then click on  . The Waveform window will show up.

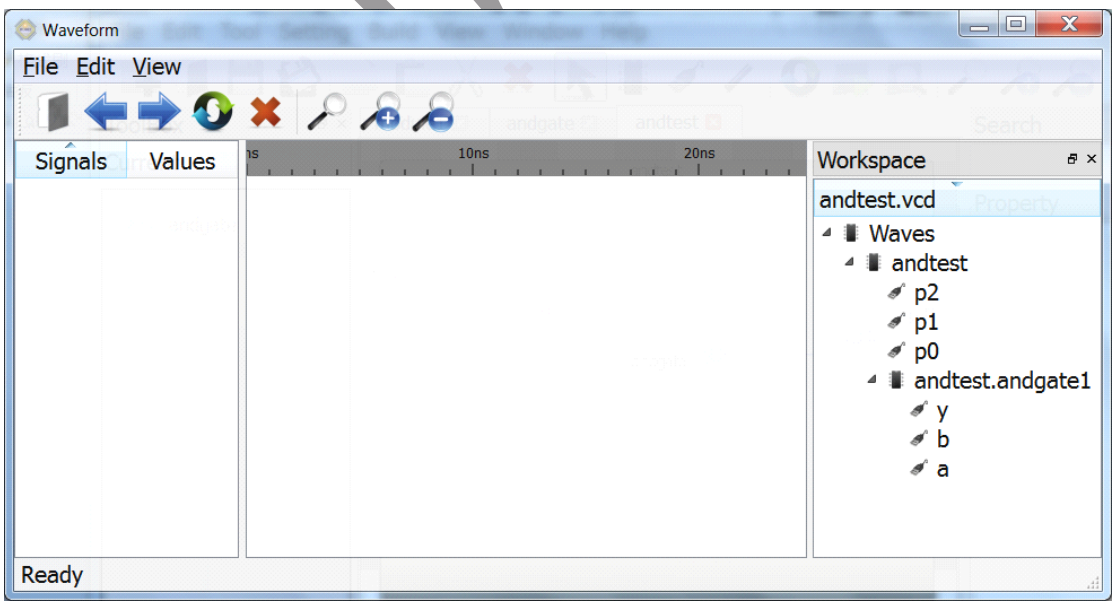


Fig. 15. Waveform window

Copyright © Robei

Click on signals listed in Workspace, add to wave window. Press  on toolbar of this window, it will zoom full of the wave. Analyze the waveform result and compare with your lab requirement.

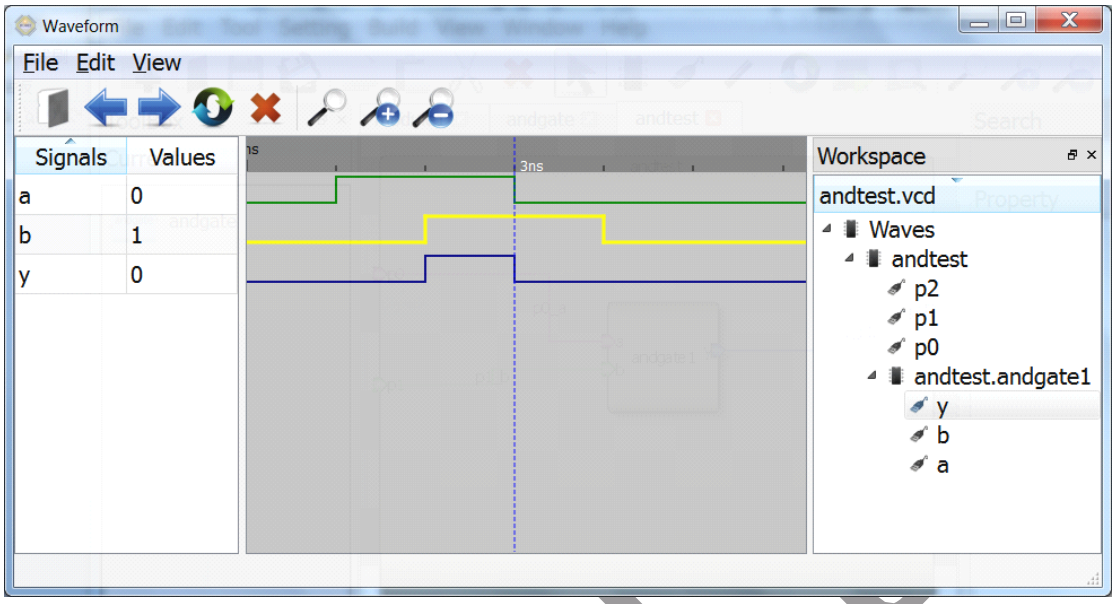


Fig. 16. Check waveform

4.Questions

In this lab, we use AND gate as an example, how can you design OR gate, Not gate and XOR gate using similar procedure? Design testbench for each of your design to verify the simulation result?

Logic gate	Symbol	Verilog code
AND	&	assign y=a&b;
OR	|	assign y=a|b;
XOR	^	assign y=a^b;
NOT	~	assign y=~a;

5. FAQ

(1). How can I see waveform from the design?

Robei has three types for each module: “module”, “model”, “testbench”. If you want to simulate and see waveform, the top module type should be changed to “testbench”. At the same time, the input port type should be “reg” and output port type should be “wire”.

(2). What is the different between model and module?

Under design module has the type of “module”, once your design finished, you can use it at any other modules. When this module used by other modules, it becomes “model”. “Model” has some properties can not be modified.

Robei LLC

(3). How can I find all the code for current design?

In "Code" tab, you can only view user input code, and that code is not start from line 1. In order to see complete code, you need go to menu: "View"-> "CodeView".

(4). Can I use simulation function without registration?

Yes but with limited designs.

Robei LLC

Copyright © Robei